REMARKS

Applicant is in receipt of the Office Action mailed February 26, 2004. Claim 1 has been amended. Claims 1, 3-7, and 9-42 are pending in the application. Further consideration of the present case is earnestly requested in light of the following remarks.

Section 102 Rejection

Claims 1, 3-7, and 9-30 stand rejected under 35 U.S.C. as being anticipated by von der Wense (U.S. Patent Number 6,598,107). Von der Wense discloses a method of communicating data between at least two units on a serial bus in a car, wherein the units have independent clocks, the data being transmitted as a sequence of frames, each frame including an identifier field and a data field.

As the Examiner is certainly aware, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Amended claim 1 recites:

1. A system for interfacing a host computer to a Controller Area Network (CAN) bus, the system comprising:

a memory configured to store program code;

an embedded processor coupled to the memory, and configured to execute the program code;

bus interface logic coupled to the embedded processor, wherein the bus interface logic is operable to couple to an interconnecting bus, wherein the bus interface logic is adapted to interface with a peripheral device through the interconnecting bus;

CAN interface logic coupled to the embedded processor and adapted for interfacing with the CAN bus;

wherein the embedded processor is operable to execute the program code to perform a CAN event in response to said bus interface logic receiving a trigger signal on the interconnecting bus from the peripheral device; and

wherein, in response to receiving the trigger signal, the embedded processor is operable to perform the CAN event substantially synchronously with an event performed by the peripheral device.

The Examiner argues that von der Wense discloses that two buses are used. Applicant respectfully disagrees. The Examiner refers to devices and their connections to the embedded processor, such as "actuators, sensors, etc. [which] are combined with a corresponding microcontroller" and "local data... are processed in the local microcontroller of the unit" (col. 1, lines 21-25). The Examiner argues that this combination and the subsequent processing establishes an interconnecting bus, and distinguishes it from a bus established by the subsequent need of "communicating data between the units" (col. 1, lines 28). The Examiner further argues that this is the conventional arrangement and use of a CAN bus, stating: von der Wense discloses that the communication hitherto associated with individual control lines between the aforementioned devices is accomplished by this additional bus system, where the embodiment preferred by von der Wense is the CAN bus, which "provides the communication backbone in up to date cars" (col. 1, lines 28-33).

Applicant respectfully disagrees with equating the connections between sensors and the corresponding microcontroller of the unit of von der Wense with the interconnecting bus of claim 1. Applicant notes that the connections between sensors and corresponding CAN devices are inherent in the Applicant's system. For example, as seen in Figure 3 of the Application, each of the CAN devices 116A – 116N may include connections to sensors, actuators, and other devices. The Specification on page 7 recites:

> "CAN interface 104 couples to a controller area network (CAN) bus 112. One or more CAN devices 116A-N may be connected to the CAN bus 112. A CAN device may represent a sensor, an actuator, or a group of sensors and/or actuators. CAN interface 104 and the CAN devices 116A-N exchange data

through the CAN bus 112 by means of packets which are commonly referred to as CAN frames.

CAN devices 116A-N interact with a physical system or unit under test (UUT) 120, i.e. receive physical signals from physical system 120 and/or assert physical signals into/onto/through physical system 120. Thus, devices 116A-N may be positioned proximate to physical system 120.

Physical system 120 may represent any physical system which is desired to be controlled, measured, analyzed, etc., or a combination of such physical systems. In one application, the physical system is automobile related. For example, the physical system 120 may be an automobile brake system, ignition system, fuel system, air conditioning system, etc., or a combination thereof. In one embodiment, the physical system 120 may represent a unit under test (UUT)."

In other words, the connections between the CAN devices and the sensors and/or actuators are inherent in a CAN system. Specifically, claim 1 includes an interconnecting bus in addition to the inherent connections between the CAN device and sensors and/or actuators. The Application describes the interconnecting bus on page :

"As discussed further below, CAN interface 104 and peripheral device 106 are coupled through an interconnecting bus (e.g. a Real-Time System Integration bus), thereby enabling substantially real-time communication between them. The interconnecting bus enables the CAN interface 104 and peripheral device 106 to send synchronizing (i.e. trigger) signals to each other, and thus, supports the synchronization of the data processing/transfer activities of CAN interface 104 and peripheral device 106. "

In other words, the interconnecting bus is used to synchronize CAN events and events of the peripheral device. This is substantially different from connections between sensors and CAN devices of von der Wense.

Moreover, claim 1 recites a peripheral device that is operable to trigger execution of a CAN event by sending the trigger signal over the interconnecting bus. The interconnecting bus is substantially different from the connections between the CAN

devices and the actuators and/or sensors. As mentioned *supra*, the CAN bus of claim 1 inherently contains connections between the CAN devices and the actuators and/or sensors by the virtue of the CAN bus. In fact, the article by Mr. Jim Pinto quoted by the Examiner also discloses sensors and actuators near distributed I/O modules in the description for Figure 2:

> "Figure 2 : Control system based on networked single- point, autonomous-I/O modules. The input modules are near the sensors, and the outputs near the actuators. "

Therefore it is well known to connect sensors to the CAN devices, i.e., I/O modules. In fact, as Mr. Pinto points out in his article, one of the purposes of a distributed I/O system is to provide local connections to sensors and/or actuators using distributed I/O devices. In contrast, the interconnecting bus connects a peripheral device to the CAN interface logic. The CAN interface logic operates to interface a host computer to the CAN bus.

Therefore it is not proper to equate the connections between the CAN device and sensors to the interconnecting bus of claim 1.

For at least the above reasons, Applicant submits that von der Wense does not teach or suggest all of the features and limitations of independent claims 1, 7, 14, 19, and 24, and thus claims 1, 7, 14, 18, 19, and 24 and those claims dependent thereon, are patentably distinct over von der Wense and are thus allowable.

Thus, Applicant submits that the present claims are allowable over the von der Wense reference. Removal of the section §102 rejection of claims 1, 3-7, and 9-30 is respectfully requested.

Section 103 Rejection

Claims 1, 3-7, and 9-42 were rejected under 35 U.S.C. 103(a) as being unpatentable over Rao (US 2003/0028701, "Rao") in view of von der Wense (US 6598107, "von der Wense"), and further in view of Pinto ("networked, intelligent I/O, the truly distributed control revolution", ISA Proceedings, December 1999, "Pinto"). Applicant respectfully disagrees.

As held by the U.S. Court of Appeals for the Federal Circuit in Ecolochem Inc. v. Southern California Edison Co., an obviousness claim that lacks evidence of a suggestion or motivation for one of skill in the art to combine prior art references to produce the claimed invention is defective as hindsight analysis.

In addition, the showing of a suggestion, teaching, or motivation to combine prior teachings "must be clear and particular . . .. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence'." *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). The art must fairly teach or suggest to one to make the specific combination as claimed. That one achieves an improved result by making such a combination is no more than hindsight without an initial suggestion to make the combination.

The Office Action asserts that Rao discloses a memory configured to store program code and an embedded processor configured to execute the program code, bus interface logic coupled to the embedded processor, adapted to interface with a device, local I/O bus interface logic and the processor operable to execute the program code to perform an event in response to the bus interface logic receiving a trigger signal on the interconnecting bus from the device, citing paragraph 19, and figure items 100, 142, and 166. The Office Action further asserts that it would have been obvious to use the CAN bus disclosed by von der Wense as the local I/O bus of Rao, as exemplified by Pinto, to produce the features and limitations of claim 1 (and the other independent claims). Applicant respectfully disagrees.

In the last Office Action the Examiner argues that an event is performed on the monitored bus of Rao and that this event occurs substantially synchronously. Furthermore, the Examiner notes that "any distinction from the synchronization of Rao must be positively recited in order to receive consideration." The Applicant respectfully notes that Rao discloses a way to synchronize two or more clock rates that may be on different buses on an IC chip, whereas claim 1 discloses an embedded processor that is operable to perform the CAN event substantially synchronously with an event performed by the peripheral device in response to receiving the trigger signal via the interconnecting bus. For example, Rao discloses a system operable to synchronize events for integrated circuits that may occur in one clock domain with another clock domain by counting events:

> [0015] As summarized above, an embodiment of the invention is an integrated circuit (IC) data processor having a number of programmable event counters for counting occurrences and durations that are internal to the data processor. The counters are part of an on-chip monitoring facility that allows the system developer to optimize a multiple bus computer system in which the data processor is being used. A die containing the on-chip monitoring facility is not a test die.. Rather, the monitoring facility is a part of every production chip. Monitoring software may be developed that accesses the counter registers via the internal bus to obtain event data related to any one of a number of buses to which the data processor is coupled. Using such software, the computer system containing the production chip may then be tuned for a particular application (e.g., network server or storage) without requiring the installation of a significant amount of additional hardware. Also, allowing bus access to memory mapped counter registers permits the use of existing programming techniques in writing the monitoring software. An efficient logic circuit is also disclosed for monitoring multiple clock domains running at different clock frequencies."

> "[0037] In the particular embodiment of FIG. 6, the qualifier circuits 604 and 608 are designed to provide a qualifier pulse signal to synchronize events occurring in the A and B clock domains with events occurring in the C clock domain. Events

in the C clock domain are generated based on a clock signal having a frequency greater than or equal to the clock signal frequencies in both the A and B clock domains. The event counters 166.sub.i are clocked by the fastest clock signal, namely the C clock in this embodiment. As can be appreciated by referring to the timing diagrams in FIGS. 7-9 below, the qualifier circuit 604 allows events in the A clock domain to be properly counted by a synchronous counter having a clock signal frequency that is higher than the A clock signal frequency. Thus, each event counter 166 is able to properly count events in the A and B clock domains using a relatively space-efficient logic circuit that includes the A and B qualifier circuits 604 and 608 and a series of AND gate 616."

In other words, Rao discloses a system for monitoring and optimizing performance of two or more buses on an integrated circuit (IC) using structures such as event counters. This is significantly different from performing a CAN event on the CAN bus triggered by an event from an interconnecting bus.

Furthermore, the Applicant respectfully disagrees with the Examiner's argument for motivation for combining the references of Rao, Pinto, and van der Wense. As mentioned *supra*, Rao does not teach or suggest synchronization events on two buses in response to triggering. Furthermore, Rao does not teach or suggests using synchronization for a distributed I/O bus such as CAN. Rather, Rao teaches monitoring and synchronization of events from two or more separate clock domains in an IC. This is significantly different from performing a CAN event on the CAN bus triggered by an event from a peripheral device over an interconnecting bus.

Furthermore, Pinto does not teach or suggest using an interconnected bus and a distributed I/O bus, such as a CAN bus. Therefore Pinto does not teach nor suggest performing a CAN event on the CAN bus triggered by an event from an interconnecting bus. Applicant submits that neither Rao, Pinto, nor van der Wense provides a motivation to combine, and further submits that even in combination, the cited references do not produce Applicant's invention as claimed.

Similar arguments apply with equal force to the 103 rejection of claims 7, 14, 19, 24, 31, and 37. Applicant thus respectfully submits that each of the independent claims 1, 7, 14, 19, 24, 31, and 37, and claims dependent thereon, are patentably distinct over the cited art, and are thus allowable. Thus, Applicant respectfully requests that the section 103 rejection of claims 1, 3-7, and 9-42 be removed.

Applicant also asserts that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant submits the application is now in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-22400/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☒ Notice of Change of Address

☒ Request for Continued Examination

Respectfully submitted,

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